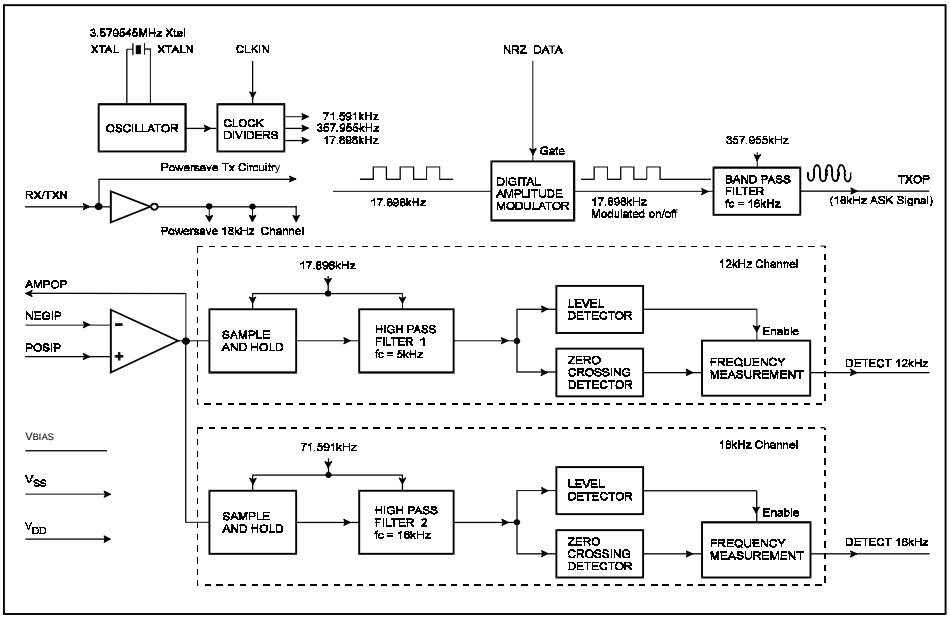
CML Semiconductor Products

SPM and Security Subsystem FX651

D/651/4 September 1997
Provisional Information

1.0 Features

- **Two Integrated Telecoms Functions:**
  - **12kHz SPM Detector**
  - **Half Duplex 18kHz Modem**
- **Compact 16-pin Small Outline (SOIC) Package**
- **Card Operated Telephone Installations**
- **Low Power (3.3V) Requirement**
- **Component Adjustable Input Sensitivity**
- **Meets European 12kHz SPM Frequency Specifications**
- **Worldwide Pay-Phone Applications**



1.1 Brief Description

The FX651 integrated circuit combines 12kHz Subscriber Private Metering (SPM) detection with 18kHz tone processing for anti-fraud purposes within a telephone system. This compact, low power device is suitable for battery or line powered systems. Under simple logic or µProcessor control it will:

Decode 12kHz SPM pulses in the presence of high level voice and 18kHz signalling, and provide a logic output.

Transmit an NRZ modulated 18kHz security tone to line.

Decode an incoming modulated 18kHz security tone in the presence of high level voice and 12 kHz SPM tones, and provide a logic output.

Employing high accuracy switched capacitor filters, the FX651 is protected from crosstalk and false decoding.

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1.2 Block Diagram

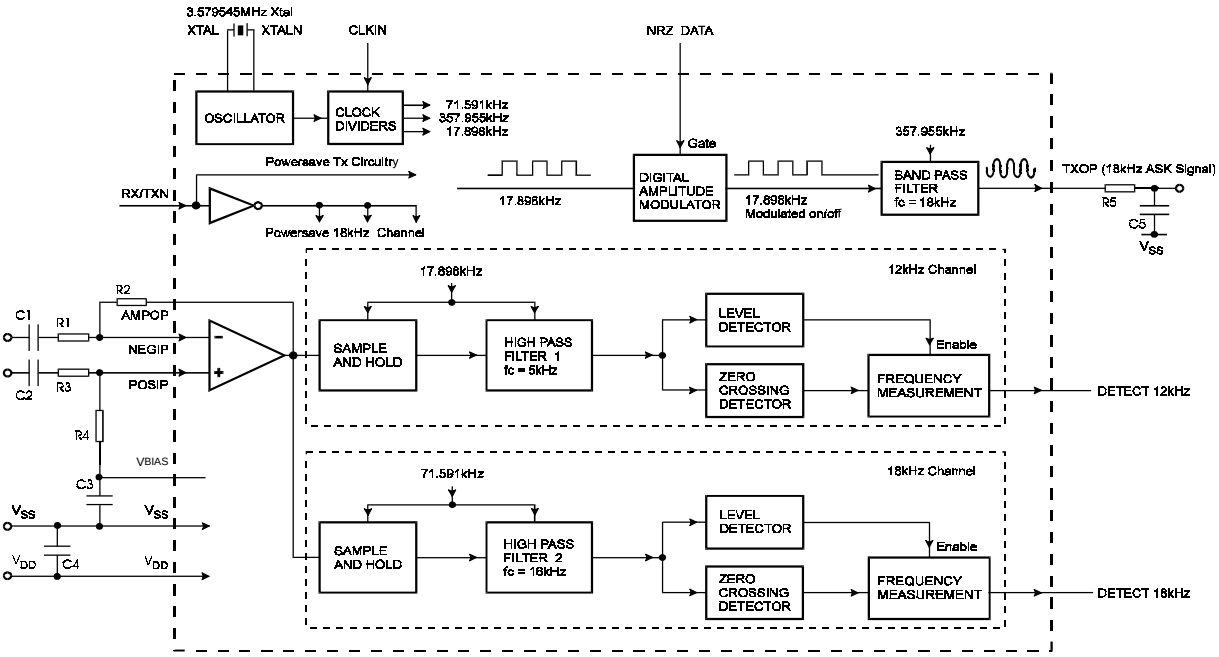


Figure 1 Block Diagram

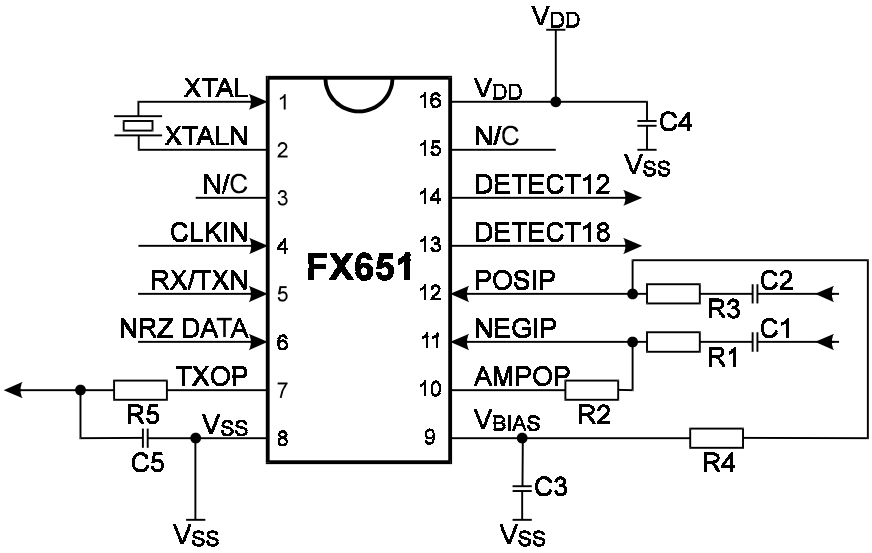
1.3 Signal List

Package D4	Signal		Description
Pin No.	**Name**	**Type**	
1	XTAL	I/P	The input to the on-chip oscillator inverter.
2	XTALN	O/P	The inverted output of the on-chip oscillator. To use, a crystal of frequency 3.579545MHz should be connected between these two pins. No other external components are necessary.
4	CLKIN	I/P	A logic input which may be used when an external clock signal is available in place of a crystal. The external 3.579545MHz signal is applied to this pin and XTAL is tied to V_{DD}. When not used, this pin should be tied to V_{DD}.
5	RX/TXN	I/P	A logic input which controls the operating mode of the device. In Rx, the device detects the presence of 12kHz and 18kHz tones. In Tx, the 18kHz detect function is disabled and 18kHz is transmitted from the TXOP pin modulated ON - OFF by the NRZ Data pin.
6	NRZ DATA	I/P	A logic input used in Tx mode to ASK modulate the TXOP pin. A logic high corresponds to no tone and logic low corresponds to 18kHz.
7	TXOP	O/P	The Tx mode output. It is ASK modulated by the NRZ data input pin. It transmits 18kHz or no tone depending upon the state of the NRZ data input pin. This pin goes to a high impedance state when in Rx mode.
8	V_{SS}	POWER	Negative supply rail.
9	V_{BIAS}	O/P	A bias line for the internal circuitry, held at ½ V_{DD}. It also forms the analogue ground for the input differential amplifier. This pin must be decoupled by a capacitor mounted close to the device pins (see Figure 1).

Package D4	Signal		Description
Pin No.	**Name**	**Type**	
10	AMPOP	O/P	The input amplifier's output. External components are used in conjunction with the amplifier to couple the line signal into the device. Both inputs are available to allow a differential configuration because a two wire input is assumed.
11	NEGIP	I/P	The input amplifier's inverting input.
12	POSIP	I/P	The input amplifier's non inverting input.
13	DETECT 18kHz	O/P	The logic output of the 18kHz channel which is active in Rx mode. Logic "0" signals the presence on the line of 18kHz tone within specified frequency and amplitude limits.
14	DETECT 12kHz	O/P	The logic output of the 12kHz channel. It goes to logic "0" when a 12kHz tone within specified frequency and amplitude limits has been detected for a minimum length of time.
16	V_{DD}	POWER	The positive supply rail. Levels and voltages are dependent upon this supply. This pin should be decoupled to V_{SS} by a capacitor (see Figure 1).
3, 15	N/C		No internal connection: leave open circuit.

Notes: I/P = Input
O/P = Output

1.4 External Components



Component	3.3V		5.0V
C1, C2	33pF ±10%		68pF ±10%
R1, R3	1.1MΩ ±1%		1.0MΩ ±1%
R2, R4	270kΩ ±1%		330kΩ ±1%
C3, C4		0.1µF ±20%	
R5		51kΩ ±1%	
C5		100pF ±10%	

Notes

1. The device's sensitivity is approximately proportional to its power supply (V_{DD}) voltage. The input gain must compensate for this and also prevent the input circuitry saturating. It is recommended that the amplifier components (R1 to R4, C1 and C2) are used to set the gain between -10dB (if V_{DD} is 5.0V) and -13dB (if V_{DD} is 3.3V).

Figure 2 Recommended External Components (D4)

1.5 General Description

1.5.1 Overall Function

The FX651 is a dual channel tone detector for use in the French Payphone system where 12kHz SPM and 18kHz security tones are used.

SPM (12kHz) Detector

The SPM detector channel responds to a low level (50mV) 12kHz tone in the presence of a large security tone (16kHz - 20kHz) and speech.
The device responds after a period of continuous valid tone and so recognises a valid SPM toneburst (minimum transmission duration, 75ms).
This function is permanently enabled.

Security Tone (18kHz) Detector (Rx Mode Only)

This demodulates the 18kHz ASK signal in the presence of the SPM signalling.

Security Tone Transmission (Tx Mode Only)

An 18kHz tone modulated ON - OFF by the NRZ data pin. A logic low gates the signal ON so that 18kHz is transmitted. A logic high gates the signal OFF so that no tone appears at the TXOP pin.

1.5.2 Description of Blocks

(See Figure 1)

Input Amplifier

This amplifier is connected as a differential amplifier and is used to couple the signal into the device. It also attenuates the combined speech, SPM tone and security tone to prevent its output saturating. Its signal gain should be -10dB at 5.0V supply and -13dB at 3.3V.
(See Figure 2 for recommended component values)

Sample and Hold (12kHz Channel)

This samples the input signal at 17.898kHz and creates images of the incoming frequencies. The 12kHz SPM is translated to 5.898kHz and the security tone is translated to between 978Hz and 1182Hz. This simplifies the subsequent signal processing.

Filtering and Frequency Detection (12kHz Channel)

The output of the sample and hold circuit is passed to filter HPF1. This is a switched capacitor high pass filter which amplifies the frequency shifted SPM tone (about 5.9kHz) but rejects the frequency shifted security tone (about 1kHz). The filter also rejects any speech signals present. The filter output is passed to the level detect and frequency measurement circuitry which determines the presence or absence of a valid SPM signal on the line. A valid signal sends the "DETECT 12kHz" pin to logic low.

Sample and Hold (18kHz Channel)

This samples the input signal at 71.592kHz. It is synchronised with the following high pass filter, which is a switched capacitor circuit with the same sampling rate. The sample and hold circuit stores the value of the input waveform value between sampling instants so that it is a suitable input for the filter.

Without the sample and hold circuit, speech or SPM tone components which are large compared with the security tone would interfere with the level discrimination at the filter output.

Filtering and Frequency Detection (18kHz Channel)
The output of the sample and hold circuit is passed to filter HPF2. This is a switched capacitor high pass filter which amplifies the security tone (about 16.92kHz - 19.08kHz) but rejects the SPM tone.

The filter output signal is passed to the level detect and frequency measurement circuitry which determines the presence or absence of a valid security tone on the line. A valid signal sends the "DETECT 18kHz" pin to logic low.

Clock Oscillator and Dividers
These circuits generate the internal clocks by division of the oscillator reference frequency. The crystal is connected as shown in Figure 2 without any need for other external components. When a crystal is used, the CLKIN pin should be left open circuit.

Alternatively, when a frequency of 3.579545MHz is externally available, the use of a crystal is unnecessary. The external frequency is applied to the CLKIN pin. In this case, the XTAL pin should be tied to V_{DD}.

In Tx, the dividers also generate a pulse train, frequency 18kHz, which is passed to the Tx circuitry (Gate ON - OFF and Band Pass Filter) for digital modulation and filtering.

Gate ON-OFF (Tx Only)
This circuit is a digital block. It performs ON - OFF modulation of the 18kHz pulse train generated from the crystal frequency by the digital dividers. It is controlled by the NRZ DATA pin and is used to encode NRZ data packets as pulsed 18kHz (ASK data). The modulated digital signal is passed to the Tx filter for wave shaping.

Band Pass Filter (Tx Only)
This is a 4th order band pass filter with centre frequency 18kHz. It shapes the modulated digital pulse train from the previous block into a low distortion pulsed sinusoidal waveform. The resulting signal is the system acknowledgement security tone. It is transmitted by the subscriber equipment, via the telephone link, to the local exchange.

1.6 Application Notes

1.6.1 Device Sensitivity versus V_{DD} - Input Amplifier Gain

The device sensitivity is proportional to V_{DD} because internal voltage references are derived from the power supply. This means that the input amplifier signal gain should be adjusted to compensate. Figure 2 shows components recommended for 5.0V and 3.3V operation.

1.6.2 Alias Responses - False Decodes

The FX651 is designed to work in telephone systems where certain ranges of input frequencies are expected and other ranges are not. The 12kHz SPM channel works in the presence of speech and a tone in the range 16kHz - 20kHz. The security tone detector functions in the presence of an interfering tone in the range 11kHz - 13kHz. A significant tone at other frequencies may interfere with correct decoding of valid transmissions and should be avoided.

A small range of input frequencies could cause false decoding when no valid tone has been received. This is because of the frequency shifting property of the SPM channel and the SWC filters (i.e sampled data filters) in both channels.

The alias frequencies which should be avoided are:

12kHz Channel

Input frequencies in the ranges:

5.708kHz - 6.078kHz	23.606kHz - 23.976kHz	29.718kHz - 30.088kHz
41.504kHz - 41.874kHz	47.986kHz - 47.616kHz	59.402kHz - 59.772kHz

In general, decodes may be caused by tones in the ranges:

$$((n \times 17.898) \pm (5.708 - 6.078))\text{kHz}$$

where n = 0, 1, 2, 3.....

Taking n = 1 and the minus sign represents valid SPM inputs in the range 11.82kHz - 12.18KHz. The other inputs represent false decodes. The response time and level sensitivity for a false decode is the same as that for a valid decode, e.g. 42ms - 45ms of 5708Hz at 50mV could cause a false decode at the "DETECT 12kHz" pin.

18kHz Channel

Input frequencies in the ranges:

52.511kHz - 54.671kHz	88.511kHz - 90.671kHz

In general, decodes could be caused by any tone in the ranges:

$$((n \times 71.591) \pm (16.92 - 19.08))\text{kHz}$$

where n = 0, 1, 2, 3.....

The case where n = 0 and the addition sign is used represents valid security tone inputs. The other cases represent false decodes. The response time and level sensitivity for a false decode is the same as that for a valid decode, e.g. 5.8ms of 52.511kHz at 40mV could cause a false response at the "DETECT 18kHz" pin.

1.7 Performance Specification

1.7.1 Electrical Performance

Absolute Maximum Ratings
Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin (wrt V_{SS})	-0.3	V_{DD} + 0.3	V
Current into or out of V_{DD} and V_{SS} pins	-30	+30	mA
Current into or out of any other pin	-20	+20	mA
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C
Total Allowable Power Dissipation at Tamb = 25°C		800	mW
Derating ...		13	mW/°C

Operating Limits
Correct operation of the device outside these limits is not implied.

	Min.	Max.	Units
Supply (V_{DD} - V_{SS})	3.0	5.5	V
Operating Temperature	-40	+85	°C
Xtal Frequency	3.579008	3.580082	MHz

Operating Characteristics
For the following conditions unless otherwise specified:

Xtal Frequency = 3.579545MHz, Noise and Distortion Measured in 50kHz Bandwidth
V_{DD} = 3.3V to 5.5V, Tamb = -40°C to 85°C.

	Notes	Min.	Typ.	Max.	Units
DC Parameters					
V_{DD}		3.3		5.5	V
I_{DD}	1		2.5	4.0	mA
I_{DD}	2		1.0	2.0	mA
Logic "1" Input Level	1, 3	3.5			V
Logic "0" Input Level	1, 3			1.5	V
Logic "1" Output Level at I_{OH} = -120µA	1	4.6			V
Logic "1" Output Level at I_{OL} = 360µA	1			0.4	V

Notes:
1. At V_{DD} = 5.0V only, I_{DD} specification does not include any current drawn from the device pins by external circuitry.
2. At V_{DD} = 3.3V only, I_{DD} specification does not include any current drawn from the device pins by external circuitry.
3. CLKIN input signal may be sinusoidal.

Operating Characteristics (continued)

	Notes	Min.	Typ.	Max.	Units
AC Parameters					
Tx Output					
Tx O/P Impedance (Tx mode)	4		1.0	2.5	kΩ
Tx O/P Impedance (Rx mode)	4	300	500		kΩ
Output Frequency		17.82		18.18	kHz
Output Distortion	5			2	%
Signal Level	5, 6	3.0	3.4	3.7	Vp-p
Signal Level	5, 7	2.0	2.2	2.4	Vp-p
Response/De-response Times	8			100	µs
Rise/Fall Times	9			5	ms
Rx Input	10				
Rx I/P Impedance		10.0			MΩ
Rx I/P Amp Voltage Gain			500		V/V
12kHz (SPM) Channel Performance	11				
With Interfering Speech & Security Tone	12				
12kHz Input Signal Level	12			800	mV
12kHz Decode Min Signal Level	12			50	mV
12kHz No Decode Max Signal Level	12	25			mV
Response Delay	12, 13	40		50	ms
De-response Delay	12, 13	40		50	ms
Detect Bandwidth	12	11.82		12.18	kHz
Not Detect Frequencies (below 12kHz)	12			11.52	kHz
Not Detect Frequencies (above 12kHz)	12	12.48			kHz
18kHz (Security Tone) Channel Performance	14				
With Interfering Speech & SPM Tone	15				
18kHz Input Signal Level	15			1.2	V
18kHz Decode Min Signal Level	15			40	mV
18kHz No Decode Max Signal Level	15	10			mV
Response/De-response Times	15, 16			8	ms
Detect Bandwidth	15	16.92		19.08	kHz
Not Detect Frequencies (below 18kHz)	15			16.25	kHz
Not Detect Frequencies (above 18kHz)	15	19.75			kHz

Notes:

4. Small signal impedance.

5. At output of smoothing network.

6. V_{DD} = 5.0V.

7. V_{DD} = 3.3V.

8. The time between a logic "1 - 0" transition at NRZ data input and the tone at TXOP reaching 10% of its full value or between a "0 - 1" transition at NRZ data input and the tone falling to 90% of its full value.

9. The time for the 18kHz tone at TXOP to rise from 10% to 90% or to fall from 90% to 10% of its full value.

10. Input amplifier signal gain set to -10dB for V_{DD} = 5.0V, -13dB for V_{DD} = 3.3V.

11. Maximum 10% distortion for incoming SPM tone, not including interfering speech or security tone (16kHz - 20kHz).
Minimum SNR 22dB for incoming SPM tone.

12. Signal levels at the line side of the input capacitor. 12kHz channel performance specified in the presence of the following interfering signals:

    (a) A 1.2V tone in the frequency range 16kHz - 20kHz.

    (b) An ordinary speech signal containing frequencies in the range 300Hz - 3400Hz of maximum instantaneous amplitude 8.0Vpk-pk.

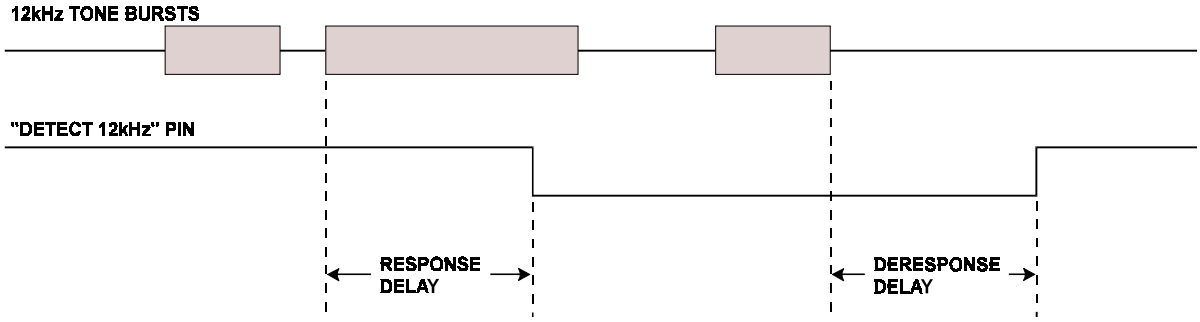
13. The device responds after 40-50ms of continuous valid tone and de-responds after: a 40-50ms period of no-tone, tones less than 25mV or an out of band tone.

14. Maximum 10% distortion for incoming security tone, not including interfering SPM tone (11kHz - 13kHz).
Minimum 20dB SNR for incoming security tone.

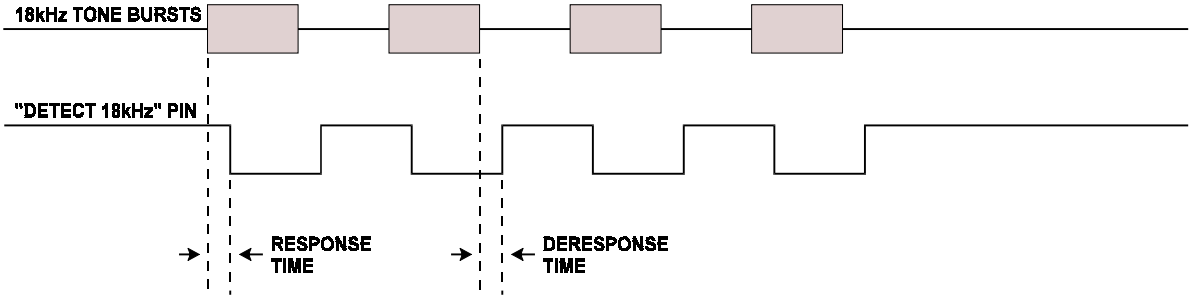
15. Signal level specified at the line side, i.e. before the input capacitor. Performance specified in the presence of an interfering 800mV tone in the frequency range 11kHz - 13kHz.

16. The device responds after 8ms of continuous valid tone and de-responds after: a 8ms period of no-tone, tone of 10mV or less, or an out of band tone.

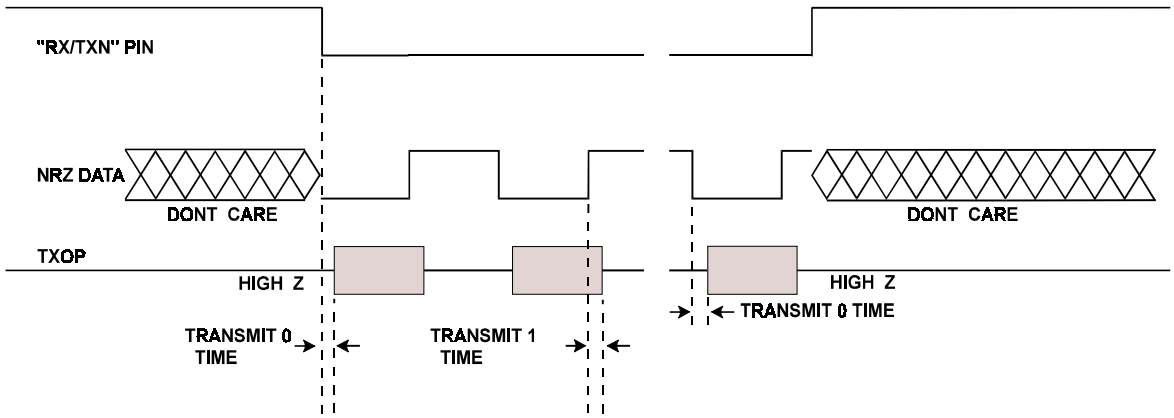
System Timings (See also Table 1 on next page)



(a) SPM (12kHz) channel. Toneburst and tonegaps less than the response and de-response delays are ignored.



(b) Security tone (18kHz) channel. The response and de-response times are short to enable the device to recognise the short ON-OFF bursts (20ms each).



(c) Transmit Mode. TXOP is modulated by the NRZ DATA pin. An 18kHz toneburst represents logic "0" and "no tone" represents logic "1". Data packets with symbol periods greater than or equal to 6ms can be transmitted.

Figure 3 System Timing Diagrams

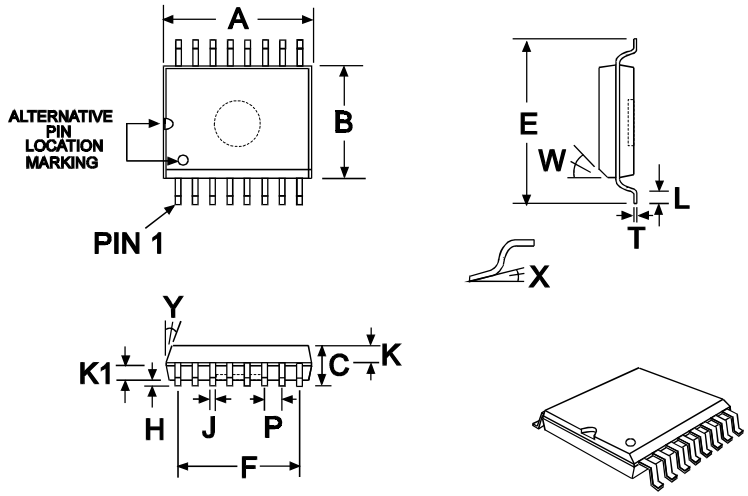
			Min	Max	Unit
Rx	12KHz	Response Delay	40	50	ms
		De-response Delay	40	50	ms
	18KHz	Response Time		8	ms
		De-response Time		8	ms
Tx *		Transmit "0" Time		5.1	ms
		Transmit "1" Time		5.1	ms

Table 1 System Timings

*** Note:** Tx Transmit Times include both Response/De-response Times and Rise/Fall Times.

1.7.2 Packaging

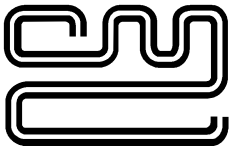
The FX651 is available in the 16-pin SOIC package detailed below:



DIM.	MIN.	TYP.	MAX.
A	0.395 (10.03)		0.413 (10.49)
B	0.291 (7.39)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.394 (10.01)		0.419 (10.64)
F		0.366 (9.29)	
H	0.004 (0.10)		0.012 (0.30)
J	0.013 (0.33)		0.019 (0.48)
K		0.041 (1.04)	
K1		0.041 (1.04)	
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.012 (0.30)
W		45°	
X	0°		8°
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles in degrees

Figure 4 SOIC Mechanical Outline: ***Order as part no. FX651D4***



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