COS/MOS 4-Word by 8-Bit Random-Access NDRO Memory

Binary Addressing CD4036AD, CD4036AK
Direct Word-Line Addressing CD4039AD, CD4039AK

Special Features:

- *COS/MOS logic compatibility at all input and output terminals*
- *Memory bit expansion*
- *Memory word expansion via Wire-OR capability at the 8 INPUT-BIT and 8 OUTPUT-BIT lines*
- *Memory bypass capability for all bits*
- *Buffering on all outputs*
- *CD4036A—on-chip binary address decoding, separate READ INHIBIT and WRITE controls*
- *CD4039A—Direct word-line addressing*
- *Access Time—200 ns (typ.) at V_{DD} = 10 V*

Applications:

Digital equipment where low power dissipation and/or high noise immunity are primary design requirements.

- *Channel Preset Memory in digital frequency-synthesizer circuits*
- *General-purpose and scratchpad memory in COS/MOS and other low-power systems.*

RCA type CD4036A is a single monolithic integrated circuit containing a 4-word x 8-bit Random Access NDRO Memory. Inputs include 8 INPUT-BIT lines, CHIP INHIBIT, WRITE, READ INHIBIT, MEMORY BYPASS, and 2 ADDRESS inputs. 8 OUTPUT-BIT lines are provided.

All input and output lines utilize standard COS/MOS inverter configurations and hence can be directly interfaced with COS/MOS logic devices.

CHIP INHIBIT allows memory word expansion by WIRE-ORing of multiple CD4036A packages at either the 8-bit input and/or output lines (see Fig. 19). With CHIP INHIBIT "high", both READ and WRITE operations are inhibited on the CD4036A. With CHIP INHIBIT "low", information can be written into and/or read continuously from one of the four words selected by the binary code on the two address lines. With CHIP INHIBIT "low", a "high" WRITE signal and a "low" READ INHIBIT signal activate WRITE and READ operations, respectively, at the addressed word location (see Fig. 4).

The MEMORY BYPASS signal, when "high", allows shunting of information from the 8 INPUT-BIT lines directly to the 8 OUTPUT-BIT lines without disturbing the state of the 4 words. During the bypass operation input information may also be written into a selected word location, provided the CHIP INHIBIT is "low" and the WRITE is "high". The READ operation is deactivated during the BYPASS operation because information is fed directly from the 8 INPUT-BIT lines to the 8 OUTPUT-BIT lines.

RCA type CD4039A is identical to the CD4036A with the exception that individual address-line inputs have been provided for each memory word in place of the binary ADDRESS, CHIP INHIBIT, and READ INHIBIT inputs. When Wire-ORing multiple CD4039A packages for memory word expansion, an individual CD4039A is selected by addressing one of its word locations. The READ operation is activated whenever a word location is addressed (via a "high" signal—see Fig. 5).

These devices will be supplied in two different 24-lead ceramic packages; the CD4036AK and CD4039AK in the flat-pack, and the CD4036AD and CD4039AD in the dual-in-line package.

MAXIMUM RATINGS,

Absolute-Maximum Values:

STORAGE-TEMPERATURE RANGE ..... −65 to +150 °C
OPERATING-TEMPERATURE RANGE ..... −55 to +125 °C
DC SUPPLY VOLTAGE RANGE ($V_{DD} - V_{SS}$) ..... −0.5 to +15 V
DEVICE DISSIPATION (Per Package) ..... 200 mW
ALL INPUTS ..... $V_{SS} \leq V_I \leq V_{DD}$
RECOMMENDED DC SUPPLY VOLTAGE ($V_{DD} - V_{SS}$) ..... 3 to 15 V
LEAD TEMPERATURE (During Soldering)
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. ..... 265 °C

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS			LIMITS CD4036AD, CD4036AK CD4039AD, CD4039AK						UNITS
		V_O Volts	V_{DD} Volts	−55 °C		25 °C		125 °C		
				Min.	Max.	Min.	Max.	Min.	Max.	
Quiescent Device Current, I_L			5	—	5	—	5	—	300	μA
			10	—	10	—	10	—	600	
Quiescent Device Dissipation/Package, P_D			5	—	25	—	25	—	1500	μW
			10	—	100	—	100	—	6000	
Output Voltage: Low-Level, V_{OL}			5	—	0.01	—	0.01	—	0.05	V
			10	—	0.01	—	0.01	—	0.05	
High-Level, V_{OH}			5	4.99	—	4.99	—	4.95	—	V
			10	9.99	—	9.99	—	9.95	—	
Threshold Voltage: N-Channel, V_{THN}	$I_D = 20\ \mu A$			1.7 typ.		1.5 typ.		1.3 typ.		V
P-Channel, V_{THP}	$I_D = -20\ \mu A$			−1.7 typ.		−1.5 typ.		−1.3 typ.		V
Noise Immunity, V_{NL} (All inputs except bit inputs when in memory bypass mode.) V_{NH}			5	1.5	—	1.5	—	1.4	—	V
			10	3	—	3	—	2.9	—	
			5	1.4	—	1.5	—	1.5	—	
			10	2.9	—	3	—	3	—	
Output Drive Current: N-Channel, I_{DN}	Normal Read Modes	0.5	5	0.12	—	0.10	—	0.07	—	mA
		0.5	10	0.30	—	0.25	—	0.17	—	
P-Channel, I_{DP}		4.5	5	−0.12	—	−0.10	—	−0.07	—	mA
		9.5	10	−0.30	—	−0.25	—	−0.17	—	
Output Drive Current: N-Channel, I_{DN}	Memory Bypass Mode +	0.5	5	0.04	—	0.03	—	0.02	—	mA
		0.5	10	0.09	—	0.075	—	0.05	—	
P-Channel, I_{DP}		4.5	5	−0.04	—	−0.03	—	−0.02	—	mA
		9.5	10	−0.09	—	−0.075	—	−0.05	—	
Input Current, I_I		—	—	—	—	10 typ.		—	—	pA

+ Bit inputs driven from low-impedance driver.

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25°C$ and $C_L = 15$ pF
Typical Temperature Coefficient for all values of $V_{DD} = 0.3\%/°C$

CHARACTERISTIC	TEST CONDITIONS		CD4036AD, CD4036AK CD4039AD, CD4039AK			UNITS
		V_{DD} Volts	Min.	Typ.	Max.	
Read Delay Time, t_{rd}: (Access time)	Output tied through 100 kΩ to V_{SS} for data output "high" and to V_{DD} for data output "low"	5	—	375	750	ns
Read Inhibit (RI)		10	—	150	300	Note 4
Chip Inhibit (CI)		5	—	500	1000	ns
		10	—	200	400	Note 4
Memory Bypass (MB)		5	—	375	750	ns
		10	—	150	300	
Address[1] (ADD)		5	—	500	1000	ns
		10	—	200	400	
Write Set-up Time[2], t_{WS}		5	250	125	—	μs
		10	100	50	—	
Write Removal Time[3], t_{WR}		5	0	0	—	ns
		10	0	0	—	
Write Pulse Duration, t_W		5	150	75	—	ns
		10	60	30	—	
Data Set-up Time[5], t_{DS}		5	—	0	0*	ns
		10	—	0	0*	
Data Overlap Time[6], t_{DO}		5	100•	50	—	ns
		10	40•	20	—	
Output Transition Time, t_{THL} / t_{TLH}		5	—	200	400	ns
		10	—	100	200	
Input Capacitance, C_I	Any Input		—	5	—	pF

1. For CD4036A only, remove 100-kΩ test condition and write all 1's in word one, and all 0's in word two, or vice versa.
2. Delay from change of ADDRESS or CHIP-INHIBIT signals to application of WRITE pulse.
3. Delay from removal of WRITE pulse to change of ADDRESS or CHIP-INHIBIT signals.
4. Values for CD4036AD and CD4036AK only.
5. The time that DATA signal must be present before the WRITE pulse removal.
   * Max. indicates satisfactory operation if t_{DS} equals or exceeds this value.
6. The time that DATA signal must remain present after the WHITE pulse removal.
   • Min. indicates satisfactory operation if t_{DO} equals or exceeds this value.

HANDLING CONSIDERATIONS

Although protection against electrostatic effects is provided by built-in circuitry, the following handling precautions should be taken:

1. Soldering iron tips and test equipment should be grounded.
2. Devices should not be inserted in non-conductive containers such as conventional plastic snow or trays.

OPERATING CONSIDERATIONS

1. Low impedance pulse generators or power supplies connected to the inputs of these devices must be disconnected before the dc power supply is turned off.
2. All unused input leads should be connected to either V_{SS} or V_{DD}, whichever is appropriate for the logic circuit involved.

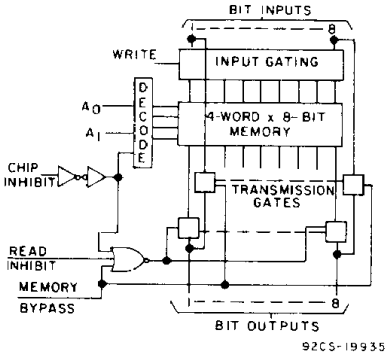


Fig. 1—CD4036A—logic block diagram.

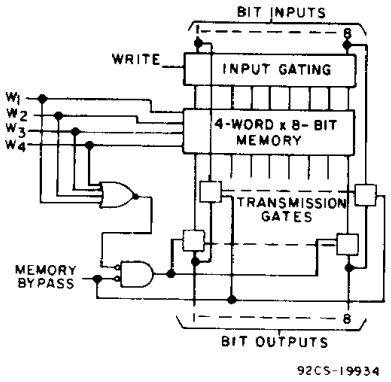


Fig. 2—CD4039A—logic block diagram.

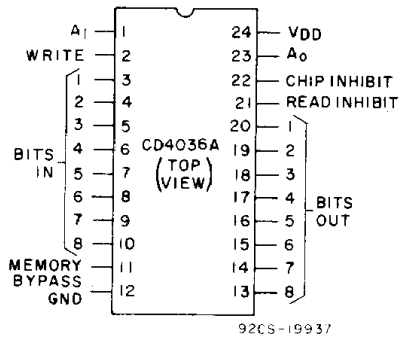
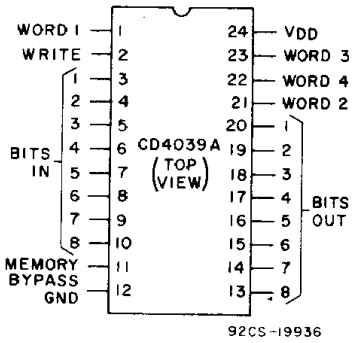


Fig. 3a)—CD4036AD and CD4036AK terminal assignments.



b)—CD4039AD and CD4039AK terminal assignments.

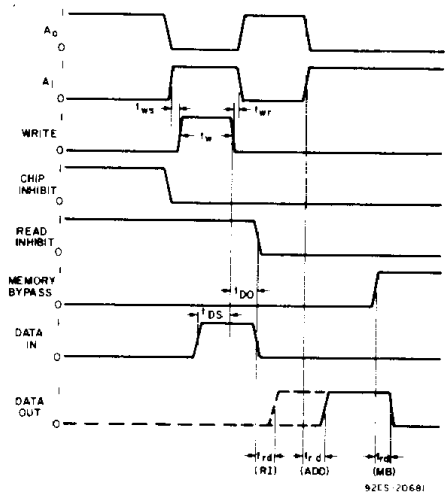


Fig. 4—CD4036A timing diagram.

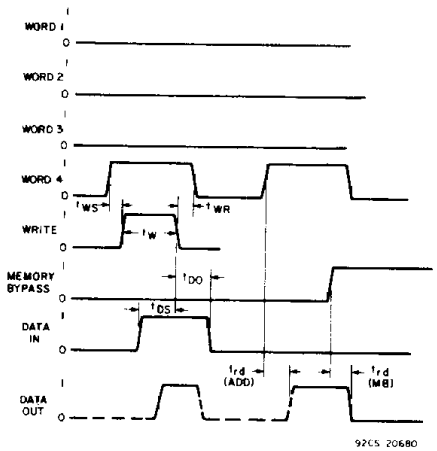


Fig. 5—CD4039A timing diagram.

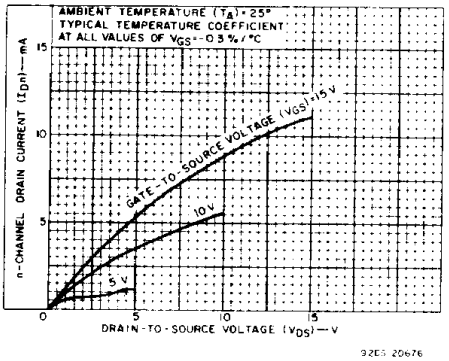


Fig. 6—Typical n-channel drain characteristics.

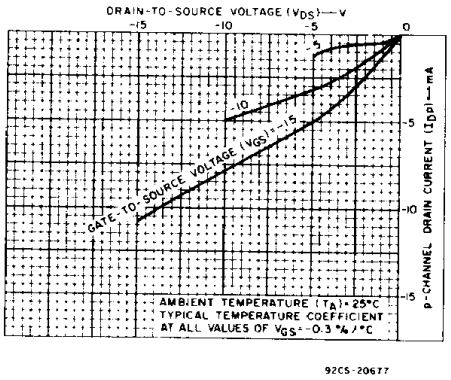


Fig. 7—Typical p-channel drain characteristics.

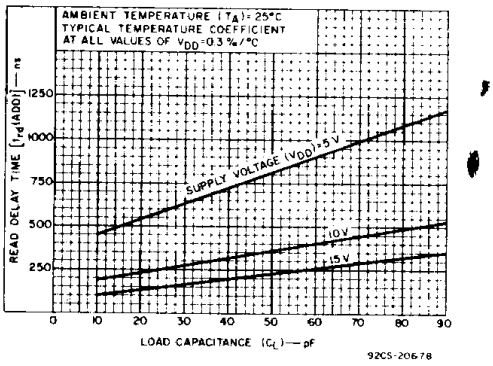


Fig. 8—Typical read delay time vs. C_L.

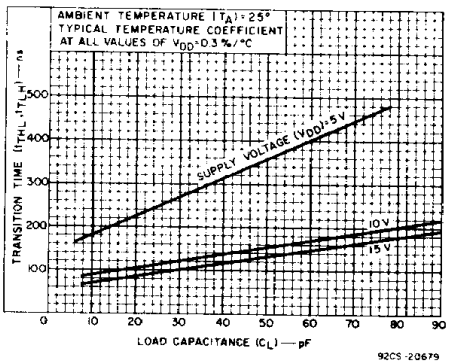


Fig. 9—Typical transition time vs. C_L.

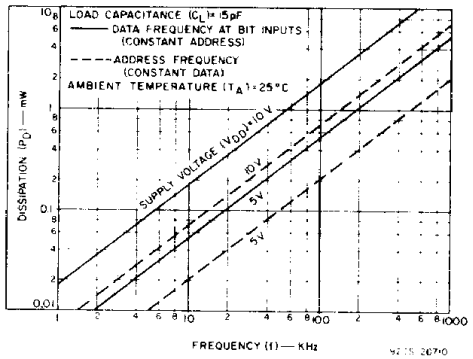


Fig. 10—Typical power dissipation vs. frequency.

TEST CIRCUITS

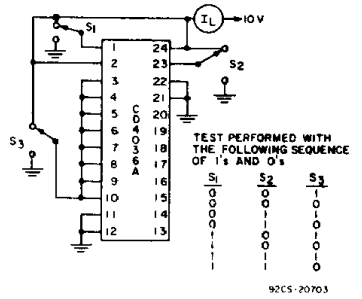


Fig. 11—Quiescent current (CD4036A).

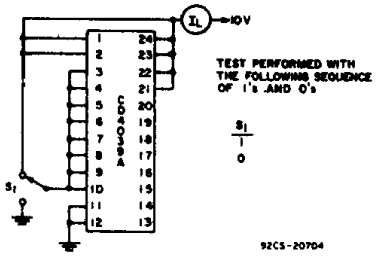


Fig. 12—Quiescent current (CD4039A).

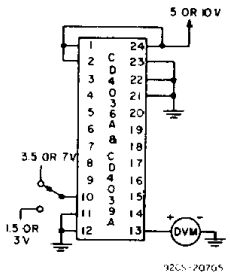


Fig. 13—Noise immunity.

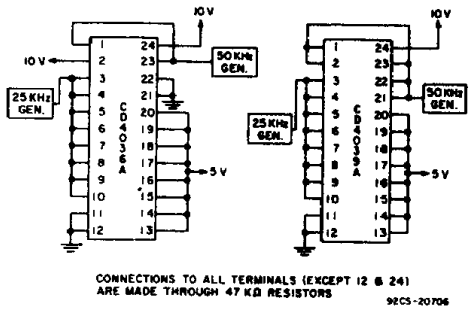


Fig. 14—Operating life.

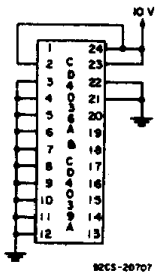


Fig. 15—Biased life.

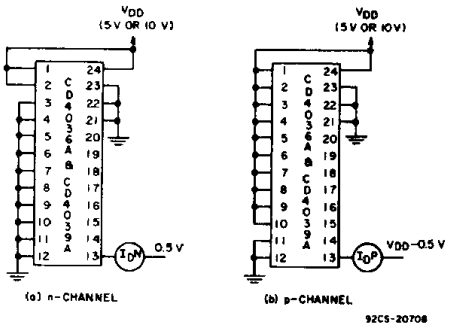


Fig. 16—Drive current.

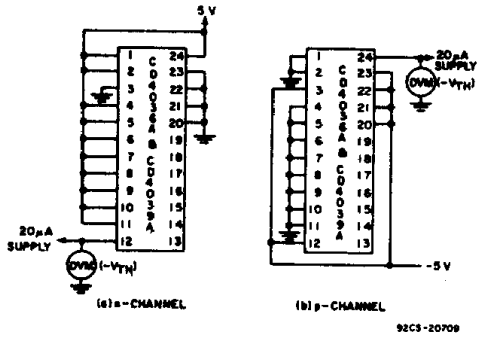
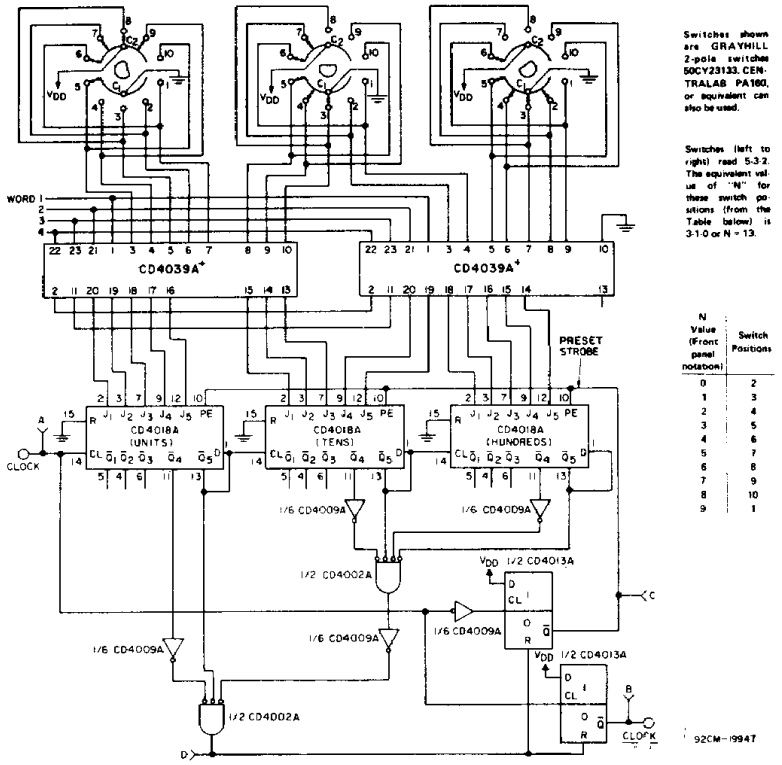


Fig. 17—Threshold voltage.



+ The CD4039A CAN BE UTILIZED IN A SIMILAR FASHION.

SEE APP. NOTE ICAN-6498 — "DESIGN OF FIXED AND PROGRAMMABLE COUNTERS USING THE RCA CD4018A COS/MOS PRESETTABLE DIVIDE-BY-'N' COUNTER" AND ICAN-6716, "LOW POWER DIGITAL FREQUENCY SYNTHESIZERS UTILIZING COS/MOS IC'S".

Fig. 18—Three-decade programmable ÷ N counter with 4-channel preset memory settings for frequency synthesizers.

The divide-by-N counter system shown in Fig. 18 is programmable from 2 to 999. Four counter-preset words, selected by means of the rotary switches, can be stored in the CD4039A devices and can be read into each CD4018A by simply addressing the proper word. Note that the CD4029A (see Bulletin File No. 503) Presettable Up/Down Counter with BCD decade counting can also be used to perform the basic counting function.

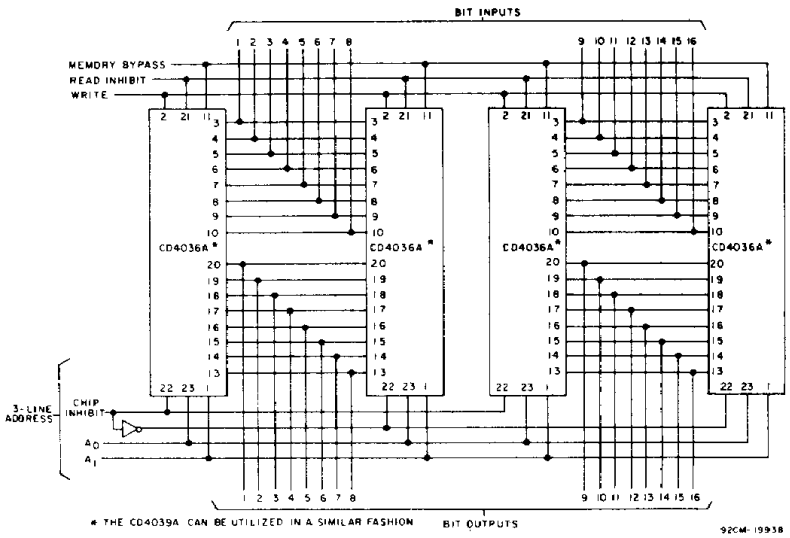


Fig. 19—General-purpose memory storage—8 words x 16 bits (RAM or ROM).