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NTE74199
Integrated Circuit
TTL – 8–Bit Universal Shift Register

Description:

The NTE74199 is an 8–bit shift register in a 24–Lead DIP type package compatible with most other TTL and MSI logic families. All inputs are buffered to lower the drive requirements to one normalized Series 74 load, and input clamping diodes minimize switching transients to simplify system design. maximum input clock frequency is typically 35Mhz and power dissipation is typically 360mW.

The NTE74199 register features parallel inputs, parallel outputs, J–$\overline{K}$ serial inputs, shift/load control input, a direct overriding clear line, and gated clock inputs nd has three modes of operation:

Inhibit Clock (Do Nothing)
Shift (In the Direction Q_A toward Q_H)
Parallel (Broadside) Load

Parallel loading is accomplished by applying the eight bits of data and taking the shift/load control input low when the clock input is not inhibited. The data is loaded into the associated flip–flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shifting is accomplished synchronously when shift/load is high and the clock input is not inhibited. Serial data for this mode is entered at the J–$\overline{K}$ inputs. See the function table for levels required to enter serial data into the first flip–flop.

Both of the clock inputs are identical in function and my be used interchangeably to serve as clock or clock–inhibit inputs. Holding either high inhibits clocking, but when one is held low, a clock input applied to the other input is passed to the eight flip–flops of the register. The clock–inhibit should be changed to the high level only while the clock input is high.

This shift register contains the equivalent of 79 TTL gates. Average power dissipation per gate is typically 4.55mW.

Absolute Maximum Ratings: (Note 1)

Supply Voltage, V_{CC} 7V
Input Voltage, V_I 5.5V
Operating Ambient Temperature Range, T_A . . . . . 0° to +70°C
Storage Temperature Range, T_{stg} . . . . . –65° to +150°C

Note 1. Voltage values are with respect to network ground terminal.

Recommended Operation Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
High−Level Output Current	I_{OH}	–	–	–800	μA
Low−Level Output Current	I_{OL}	–	–	16	mA
Clock Frequency	f_{clock}	0	–	25	MHz
Width of Clock or Clear Pulse	t_w	20	–	–	ns
Mode Control Setup Time	t_{su}	30	–	–	ns
Data Setup Time	t_{su}	20	–	–	ns
Hold Time at Any Input	t_h	0	–	–	ns
Operating Ambient Temperature	T_A	0	–	70	°C

Electrical Characteristics: (Note 2, Note 3)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
High−Level Input Voltage	V_{IH}		2	–	–	V
Low−Level Input Voltage	V_{IL}		–	–	0.8	V
Low−Level Clamp Voltage	V_{IK}	V_{CC} = MIN, I_I = −12mA	–	–	−1.5	V
High−Level Output Voltage	V_{OH}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −800μA	2.4	3.4	–	V
Low−Level Output Voltage	V_{OL}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 16mA	–	0.2	0.4	V
Input Current	I_I	V_{CC} = MAX, V_I = 5.5V	–	–	1	mA
High−Level Input Current	I_{IH}	V_{CC} = MAX, V_I = 2.4V	–	–	40	μA
Low−Level Input Current	I_{IL}	V_{CC} = MAX, V_I = 0.4V	–	–	−1.6	mA
Short−Circuit Output Current	I_{OS}	V_{CC} = MAX, Note 4	−18	–	−57	mA
Supply Current	I_{CC}	V_{CC} = MAX, See Table Below	–	90	127	mA

Note 2. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

Note 3. All typical values at V_{CC} = 5V, T_A = +25°C.

Note 4. Not more than one output should be shorted at a time.

Test Conditions for I_{CC} (All Outputs Are Open):

Apply 4.5V	First Ground, Then Apply 4.5V	Ground
Serial Input, S_0, S_1	Clock	$\overline{\text{Clear}}$, Inputs A thru H
J, $\overline{K}$, Inputs A thru H	Clock	Clock Inhibit, Clear, Shift/$\overline{\text{Load}}$

Switching Characteristics: (T_A = +25°C, V_{CC} = 5V unless otherwise specified)

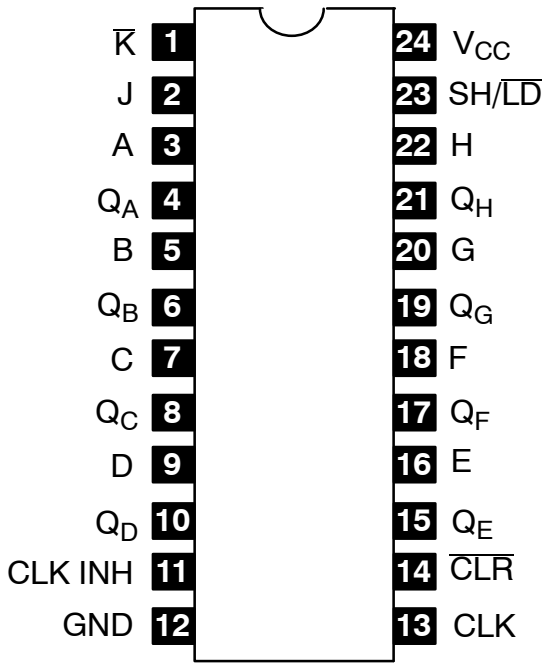
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Maximum Clock Frequency	f_{max}	C_L = 15pF, R_L = 400Ω	25	35	–	MHz
Propagation Delay Time, from Clear	t_{PHL}		–	23	35	ns
Propagation Delay Time, from Clock	t_{PHL}		–	20	30	ns
	t_{PLH}		–	17	26	ns

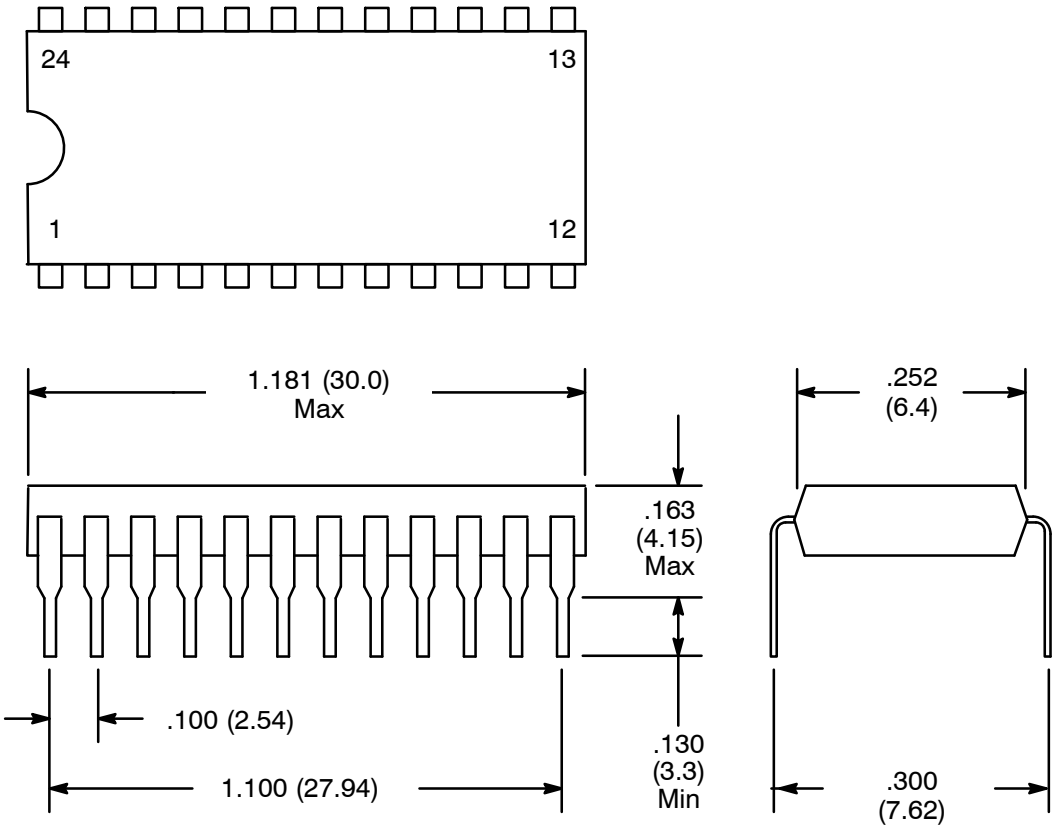
Function Table:

Inputs							Outputs				
				Serial		Parallel					
$\overline{\text{CLEAR}}$	SHIFT/$\overline{\text{LOAD}}$	CLOCK INHIBIT	CLOCK	J	$\overline{\text{K}}$	A . . . H	Q_A	Q_B	Q_C	. . .	Q_H
L	X	X	X	X	X	X	L	L	L		L
H	X	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}		Q_{H0}
H	L	L	↑	X	X	a . . . h	a	b	c		h
H	H	L	↑	L	H	X	Q_{A0}	Q_{A0}	Q_{Bn}		Q_{Gn}
H	H	L	↑	L	L	X	L	Q_{An}	Q_{Bn}		Q_{Gn}
H	H	L	↑	H	H	X	H	Q_{An}	Q_{Bn}		Q_{Gn}
H	H	L	↑	H	L	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}		Q_{Gn}
H	X	H	↑	X	X	X	Q_{A0}	Q_{B0}	Q_{B0}		Q_{H0}

H = High Level (Steady State)
L = Low Level (Steady State)
X = Irrelevant (Any input, including transitions)
↑ = Transition from low to high level
a . . . h = Then level of steady−state input at inputs A thru H, respectively
Q_{A0}, Q_{B0}, Q_{G0}, Q_{H0} = The level of Q_A, Q_B, Q_G, or Q_H, respectively, before the indicated steady−state input conditions were established.
Q_{an}, Q_{bn}, etc. = The level of Q_A, Q_B, etc., respectively, before the most−recent ↑ transition of the clock.

Pin Connection Diagram:




24
13
1
12
1.181 (30.0)
Max
.163
(4.15)
Max
.100 (2.54)
1.100 (27.94)
.130
(3.3)
Min
.252
(6.4)
.300
(7.62)